**SRM Institute of Science and Technology**

**SET B**

**College of Engineering and Technology**

**School of Computing**

**DEPARTMENT OF COMPUTING TECHNOLOGIES**

SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

**Academic Year: 2022-2023**

**Test: CLAT-1 Date: 12-9-2022**

**Course Code & Title: 18CSC203J: Computer Organization and Architecture Duration: 1 Period**

**Year & Sem: II & III Max. Marks: Marks**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Course Outcomes (CO): | | | | | | *The learners will be able to* | | | | | | | | | |
| **CO-1 :** | | *Identify the computer hardware and how software interacts with computer hardware* | | | | | | | | | | | | | |
| Program Outcomes (PO) | | | | | | | | | | | | |  | | |
| 1 | 2 | 3 | 4 | 5 | 6 | | 7 | 8 | 9 | 10 | 11 | 12 | PSO | | |
| Engineering Knowledge | Problem Analysis | Design & Development | Analysis, Design, Research | Modern Tool Usage | Society & Culture | | Environment & Sustainability | Ethics | Individual & Team Work | Communication | Project Mgt. & Finance | Life Long Learning | PSO - 1 | PSO - 2 | PSO – 3 |
| *3* | *3* |  |  |  |  | |  |  | *2* | *1* |  | *2* |  |  | |

3-High, 2- Medium, 1-low

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Question** | **Marks** | **BL** | **CO** | **PO** | **PI Code** |
| Which one of the following buses is unidirectional?   * Data bus * Control bus * **Address bus** * System bus | **1** | **1** | **1** | **1** | **1.3.1** |
| Choose the memory of the computer which is used to synchronize with a high-speed CPU there by improving its performance.   * **Cache Memory** * Main Memory * Flash Memory * Secondary Memory | **1** | **1** | **1** | **2** | **2.6.2** |
| Consider a CPU that has 64- bit, the address of the contents are 1000, 1008,  1016, 1024. Now MAR is holding an address is 1008 to fetch the content from  the memory. Analyze the operation and select the following address of the content which is held by the Program Counter (PC).   * 1000 * 1008 * **1016** * 1024 | **1** | **3** | **1** | **2** | **2.5.2** |
| Compute the number of address lines required to select 8 locations in multi-bus structure.   * 1 * 2 * **3** * 4 | **1** | **2** | **1** | **2** | **2.5.2** |
| Consider the computer uses 22 bits to address memory and 1 byte per memory location. Compute the capacity of the computer’s memory.   * 2 megabytes of memory * **4 megabytes of memory** * 6 megabytes of memory * 8 megabytes of memory | **1** | **3** | **1** | **2** | **2.5.2** |
| Solve the problem A=8, and B=6 using Bitwise AND operator and find the result of this operation.   * 1111 * 1010 * **1110** * 0101 | **1** | **3** | **1** | **2** | **2.5.2** |
| Solve the instruction ROL R1, 2 ; consider the value of R1 is 1010 1111, 2 is number of shifting and find the result after rotation.   * **1011 1110** * 1011 1100 * 1011 1111 * 1011 1101 | **1** | **3** | **1** | **2** | **2.5.2** |
| Solve the problem R1= 1100 1100 >> 3 using right shift operator, here 3 is number of shifting and find the result of this operation.   * 1001 0001 * **0001 1001** * 1100 1001 * 0011 1001 | **1** | **3** | **1** | **2** | **2.5.2** |
| Analyze the addressing modes and match with its purpose.  X. Indirect addressing - 1. Loops  Y. Immediate addressing - 2. Pointers  Z. Auto decrement addressing - 3. Constants   * X – 3, y – 2, Z – 1 * **X – 2, y – 3, Z – 1** * X – 1, y – 3, Z – 2 * X – 3, y – 1, Z – 2 | **1** | **3** | **1** | **2** | **2.5.2** |
| Consider a three-word machine instruction ADD A[R0], [B]. The first word of the instruction specifies the opcode, followed by A and B are memory addresses residing at the second and the third words, respectively. During the execution of ADD instruction, the two operands are added and stored in the destination (first operand). Compute the number of memory cycles used during the execution cycle of the instruction.   * 3 * 4 * 5 * **6** | **1** | **3** | **1** | **2** | **2.5.2** |
| Each instruction in ARM is encoded into how many words   * 2 bytes * **4 bytes** * 8 bytes * 3 bytes | **1** | **1** | **1** | **1** | **1.7.1** |
| Identify a register that does not allow the user to modify the content of the register.   * **Code Segment Register** * Data Segment Register * Extra Segment Register * Both b and c | **1** | **1** | **1** | **1** | **1.7.1** |
| Compute the allocated bytes and select the result of this instruction.   * stars DB 4 DUP (3 DUP (’\*’), 2 DUP (’?’), 5 DUP (’!’)) * 4 Bytes and \*?! * 19 Bytes and \*\*\*\*????!!!! * 34 Bytes and !!!!!!!!!!!!!!!????????\*\*\*\*\*\*\*\*\*\*\*\* * **40 Bytes and \*\*\*??!!!!!\*\*\*??!!!!!\*\*\*??!!!!!\*\*\*??!!!!!** | **1** | **3** | **1** | **2** | **2.5.2** |
| Identify the suitable instructions for memory accessing operation in ARM systems. 1. STORE 2. MOVE 3. LOAD 4. ARITHMETIC   * 1 & 2 * 2 & 4 * **1 & 3** * 2 & 3 | **1** | **2** | **1** | **1** | **1.7.1** |
| The content of the register is R1=20H, R2=35H, and R3=50H. The following machine instruction is executed.  PUSH {R1}  PUSH {R2}  PUSH{R3}  POP {R1}  POP {R2}  POP {R3}  Solve the instruction and find the content of registers R1, R2, R3 after execution.   * R1=20H, R2=35H, R3=50H * **R1=50H, R2=35H, R3=20H** * R1=20H, R2=50H, R3=35H * R1=35H, R2=50H, R3=20H | **1** | **3** | **1** | **2** | **2.5.2** |